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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 15

Application Number: 09/591,226
Filing Date: June 09, 2000
Appellant(s): BALDWIN, DAVID ROBERT

N. Elizabeth Pham
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2/6/04.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is substantially correct. The changes are as follows:

Issue 2 – Rejection of claims 2, 3, 5 and 6 under 35 USC 103(a) as being unpatentable over Porterfield in view of Mergard et al or Poirion have been withdrawn; and

Issue 3 – Rejection of claims 2, 3, 5 and 6 under 35 USC 103(a) as being unpatentable over Peddada et al in view of Mergard et al, or Popirion or Chen et al has been withdrawn.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-6 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,295,068	Peddada et al	9-2001
6,249,853	Porterfield	6-2001
6,292,201	Chen et al	9-2001

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peddada et al (6,295,068) in view of Porterfield (6,249,853).

Peddada teaches a graphics processing method (Figs. 4-6) comprising performing 3D graphics rendering in a graphics accelerator subsystem (Fig. 5, 20), using a dedicated graphics memory (22 and 24) as primary memory for rendering accelerator logic; using a system main memory (14) as additional memory to hold

textures required by said rendering accelerator logic; and when textures required by sad rendering accelerator logic are not present in said dedicated graphics memory, then either downloading said textures from main memory into said graphics memory (Fig. 5, can be download from disk 18 to AGP mem 14 to texture cache 24). However, Peddada fails to explicitly suggest or teach, selectively, when commanded by a software application, allowing said accelerator logic to read textures directly from said main memory without downloading them into said graphics memory. Peddada teaches there are two AGP models. One is known as the AGP DMA model which downloading texture data from main memory into texture cache in the graphics accelerator (col. 1, line 63 through col. 2, line 9) and another is known as AGP Execute model, has 3D graphics accelerator accessing textures from AGP memory (part of the main memory) via system logic chip over AGP bus (col. 1, lines 50-57). However, Peddada uses a different way to achieve the benefit of AGP Execute model. Porterfield also teaches two AGP models, a DMA and Execute models (col. 6, line 55 through col. 7, line 5). Porterfield teaches an AGP Execute model by add additional mapping mechanism, such as, GART which is also known to Peddada (col. 1, lines 58-62 and col. 9, lines 6-32). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Porterfield into Peddada in order to use both AGP models and thus to add the flexibility to the system. Therefore, at least claim 1 would have been obvious.

As per claim 4, Porterfield teaches said accelerator logic is able to read non-contiguous textures directly from said main memory (col. 6, line 65 to col. 7, line 5).

3. Claims 2, 3, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Porterfield (6,249,853) in view of Chen et al (6,292,201).

Porterfield teaches a graphics processing chip (Fig. 3, 160) comprising rendering acceleration chip (part of the graphics accelerator 160); and software which has a user accessible mechanism in place to do logical-to-physical mapping into a main system memory (MMU portion of the system logic 154, i.e., the same logic for both Fig. 1 and 3, and further see col. 6, lines 22-32 and col. 6, line 55 through col. 8, line 3 and Figs. 4 and 5a). However, Porterfield fails to explicitly suggest or teach the software integrated on the chip with the graphics accelerator chip. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of Porterfield into a single chip integrated circuit in order to achieve a low cost, low space system without sacrificing overall performance. Chen teaches a single chip integrated circuit that combines the graphics accelerator and system logic plus many other system components into a single chip integrated circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Chen into the system of Porterfield in order to provide a single chip integrated circuit as claimed in order to achieve the different advantages as taught by Chen (col. 3, line 35 through col. 4, line 30 and further see col. 7, lines 27-31). Therefore, at least claim 2 would have been obvious.

As per claim 5, Porterfield teaches the software is able to read noncontiguous textures directly from said main memory (col. 7, lines 21-31).

Claim 3 is similar in scope to claim 2, and additionally requires a texture memory management function, integrated on said chip, which manages both texture storage in host memory and also texture storage in normal texture memory (part of the function of the graphics accelerator, col. 6, lines 55-61).

As per claim 6, Porterfield teaches said texture memory management function is able to read noncontiguous texture directly from said main memory (col. 6, lines 61-67).

(11) Response to Argument

Regarding claim 1, appellant argues that (a) there is no motivation to modify or combine the references in a way that meets the claimed invention of claim 1. The motivation to modify or combine the references is given in the detailed rejection with respect to claim above. (b) Peddada et al teaches away from allowing the graphics accelerator direct access to the main memory because the 3D graphics accelerator 20 must have additional hardware to directly access textures from AGP memory 14. This extra hardware adds to the expense and complexity of 3D graphics accelerator 20 and is thus undesirable. Well, as point out by Appellant that Peddada suggests in the background of invention that the graphics accelerator can access textures "***directly***" from main system memory in AGP Execute model by add extra hardware. It is noted that "directly" means the graphics accelerator can access or execute the texture data in the main memory without copy to the local texture memory. Therefore, at least from the suggestion of the background of invention, the invention is well known and obvious to Peddada et al (as prior art). Prior art reference that "teaches away" from claimed

invention is significant factor to be considered in determining unobviousness, but nature of such teaching is highly relevant, and must be weighed in substance; known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for same use. ***In re Gurley*** 31 USPQ2d 1130 (CAFC 1994).

Regarding claim 4, Appellant argues that Porterfield fails to teach an accelerator logic that is capable of reading non-contiguous textures directly from the main memory because Porterfield requires an address mapping mechanism in execute model. However, the reading by the accelerator logic of Porterfield is still considered a directly because the meaning of "directly" here is meaning reading or execute from main memory without copy to the local texture memory.

Regarding claim 2, Appellant argues that the prior art fails to teach "software, integrated on said chip, which has a user accessible mechanism in place to do logical-to-physical mapping into a main system memory." And there is no motivation to modify or combine the references in a way that meets the claimed invention of claim 2. The examiner disagrees. As point out in the detailed rejection above, Porterfield teaches the claimed software (see col. 7, lines 21-31) performs by system logic 154 which is not integrated into the graphics chip. Chen teaches an integrated system logic chip which integrated graphics accelerator and a chipset into a single IC which shows/proves that the graphics accelerator 160 and system logic 154 can be combined. Because the software is performed by system logic 154, thus the combination also teaches integrated software (by system logic 154) into graphics accelerator 160. Regarding the

teaching of a user accessible mechanism, it is well known that a software is user accessible at least to a programmer (user) because the programmer can program or reprogram the software.

There is no particular argument regarding claim 5.

Regarding claim 3, appellant argues that accessing memory is not the same as managing memory. Well, without recited any particular functions of memory managing in the claim to distinguish from memory accessing of Porterfield, the teachings of accessing memory by Porterfield can be considered as memory managing because accessing memory is one of memory managing functions.

Regarding claim 6, appellant argues that Porterfield fails to teach a graphics accelerator chip includes a memory management function. The examiner disagrees again. As discussed above, the graphics accelerator and system logic can be combined as a single chip and thus the MMU performing by system logic 154 can be considered as part of the functions of graphics accelerator.

All the arguments have been addressed in detailed above.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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Primary Examiner
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KMT
March 4, 2004

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